

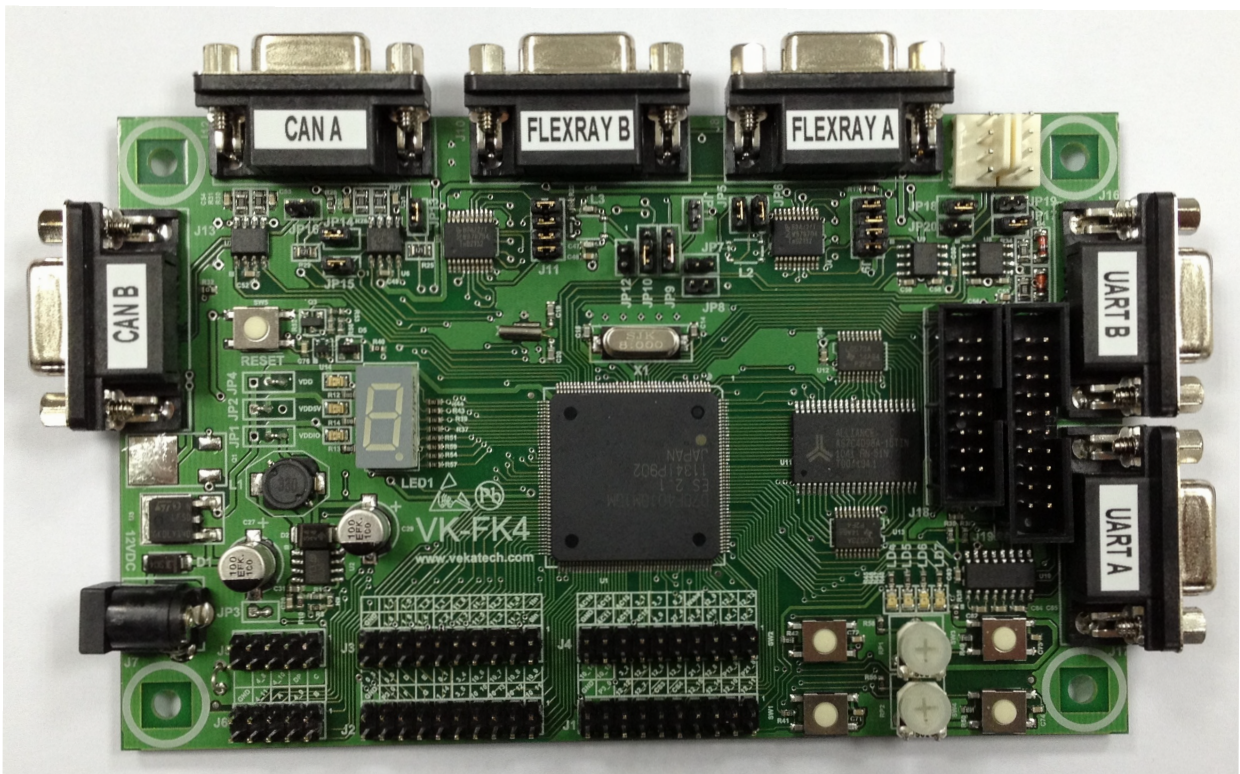
VK-FK4 Development Board

User Manual

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The document is intended to guide users with background in embedded systems to use VK-FK4 Development Board in their applications.

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Chapter 1: Introduction

VK-FK4 is a development board, which uses MCU uPD70F4010 from Renesas Electronics. This 32bit powerful MCU supports various serial interfaces such as FLEXRAY, CAN, UART/LIN, SPI, etc.. In addition, you will find also 20 pins N-WIRE debugging interface for Minicube2. On the board 256k x 16bit SRAM. User push buttons and LED's and 7 Seg LED indicator. All this, along with the DC/DC power supply on board and connected to pin headers, unused pins of uPD70F4010, allow you to build a diversity of powerful applications, which could be used in a wide range of embedded tasks.

1.1 Main features of VK-FK4

- ⌚ MCU: V850E2M FK4 – uPD70F4010
- ⌚ 2-FlexRay interfaces (TLE6250G)
- ⌚ 2-CAN interfaces (TLE6250G)
- ⌚ 2-LIN interfaces(ZMD30011)
- ⌚ SRAM 512kB (AS7C4098A-12TCN)
- ⌚ 20 pins Debug Minicube connector.
- ⌚ User 4 LEDS and 7 segment LED.
- ⌚ User 4 push buttons and RESET button.
- ⌚ Power connector for DC/DC 7V-15V
- ⌚ FR-4, 1.6 mm, Green/White solder mask, component print.
- ⌚ Dimensions: 142.11mm x 88.77mm

1.2 Electrostatic warning

The VK-FK4 board is shipped in protective anti-static packaging. The board must not be subject to high electrostatic potentials. General practice for working with static sensitive devices should be applied when working with this board.

1.3 Processor Features

The VK-Jx3-E board use 32bit V850E2-FK4 MCU uPD70F4010 from Renesas Electronics with the following features:

ROM: 2048 KB Flash
 Data Flash: 64 KB
 RAM: 144 KB
 Backup RAM: 16 KB
 Operating Voltage: 3.0 V to 5.5 V
 Max. Frequency: 80 MHz
 Package: 176 HQLFP
 V850E2M CPU core
 System Protect Function (SPF): MPU, SRP, TSU, PPU
 Instruction Cache 8 KB (2-way)
 DMA: 8 channels
 Main oscillator : 4 to 20 MHz

Low speed internal oscillator: 240 kHz typ.

High speed internal oscillator: 8 MHz typ.

Sub clock: 32.768 Hz typ.

PLL: 80 MHz max.

I/O port: 72

A/D Converter: 24 channels

Timers :

- ⌚ Timer Array Unit A: 16-bit x 1 unit x 16 channels
- ⌚ Timer Array Unit B: 16-bit x 1 unit x 16 channels
- ⌚ Timer Array Unit C: 16-bit x 5 units x 16 channels
- ⌚ Timer Array Unit J: 32-bit x 2 units x 4 channels
- ⌚ Window watchdog timer: 2 channels
- ⌚ OS timer: 1 channel
- ⌚ Motor control timer: 1 channel
- ⌚ Encoder timer: 1 channel

Serial Interface :

- ⌚ CAN: 64 message buffer x 3 channels, 128 message buffer x 1 channel .
- ⌚ LIN-UART: 8 channels
- ⌚ CSI: 2 channels
- ⌚ CSI with FIFO: 3 channels
- ⌚ I2C: 1 channel
- ⌚ Flexray : 1 unit : 2 channels

Interrupt:

- ⌚ Maskable: External 16
- ⌚ Non Maskable: External 1

Power on Clear

Power source comparator: 2 channels

Clock monitor: Main cleck, high speed internal oscillator, PLL0 available

Random number Generator: 1 channel

Data CRC: 1 channel

Key interrupt: 8 channels

Wake up signal output

FOUT Available

On-chip debugg function

Operating temperature:-40 to +125°C

For more information, please visit www.renesas.eu

1.4 System requirements

Host PC: A PC for the the IAR Systems Embedded Workbench demo-version supporting Windows 2000, Windows XP or Windows Vista is required.

Adobe Acrobat Reader.

1.5 Package contents

VK-FK4 board.

3M glue legs.
N-WIRE to E1 Debbuger converter board and flat cable.
CD with demo projects.

1.6 Trademarks

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Chapter 2: VK-FK4 System Configuration.

VK- FK4 can be used in general Flexray,CAN,LIN,UART and SPI, communications environment and other embedded task as motor control etc.

2.1 Power supply circuit

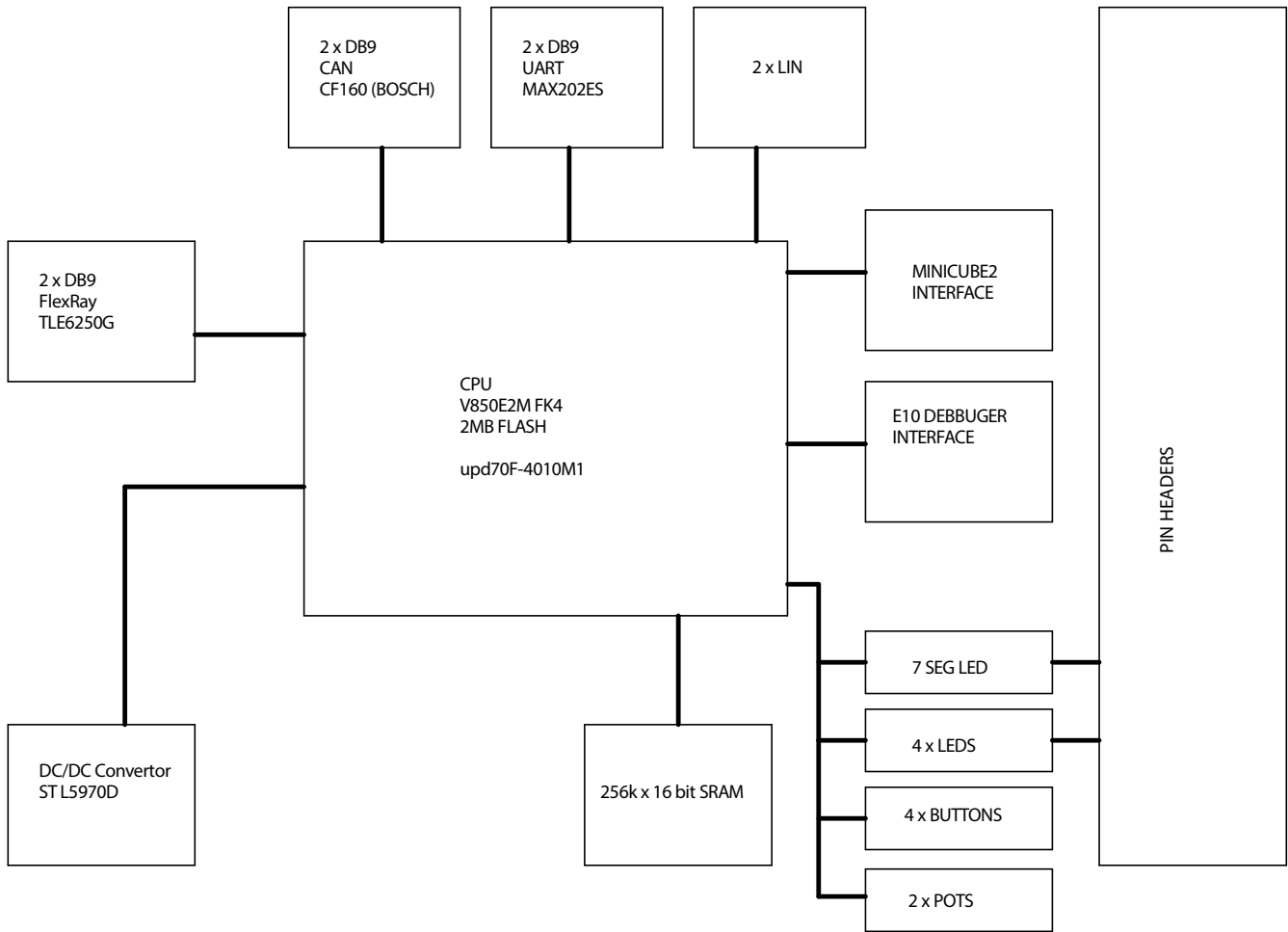
VK- FK4 is supplied by one of the following interfaces listed below.
Power consumption may varies and the maximum is **40** mA.

Via DC Power Adapter

VK-FK4 is powered by (7-15) VDC applied at the power jack J7

Chapter 3: Hardware

3.1 Block Diagram



3.2 Hardware Components

3.2.1 Clock Circuits

Quartz crystal 8.0000 MHz is connected to uPD70F4010 21(X1) pin and pin(X2) 20.
 Quartz crystal 32.768KHz is connected to 25(XT1) pin and 24(XT2) pin.

3.2.2 External SRAM Base Addresses

SRAM 256k x 16bit (AS7C4098A-15TCN).
 xRAM : ORIGIN = 0x00400000, LENGTH = 256k.
 No additional wait cycles required.

3.2.3 LED's:

Component	NET name	MCU pin
LD4	P12_10	143 pin (upd70F4010)
LD5	P12_11	144 pin (upd70F4010)
LD6	P12_14	147 pin (upd70F4010)
LD7	P12_15	148 pin (upd70F4010)

3.2.4 7 SEG LED:

Signal Name	Pin name	Pin #
LED 7SEG A	P4_7	50
LED 7SEG B	P4_6	51
LED 7SEG C	P4_5	52
LED 7SEG D	P4_2	55
LED 7SEG E	P4_0	57
LED 7SEG F	P4_3	54
LED 7SEG G	P4_1	56
LED 7SEG DP	P4_4	53

3.2.5 Push buttons:

Comp	Signal name	MCU_pin	Pin Heared
*SW1	P21_7		
*SW2	P21_8		
*SW3	P12_8		
*SW4	P12_9		
RESET	Reset Driver Input		MCU pin
SW5	2		6

3.2.6 Connectors Description:

PWR

Pin#	Signal Name	Pin#	Signal Name
1	Positive power	2	Negative power

The power input should be +(7-15VDC)

N-WIRE interface - 20 pins connector J19:

Pin#	Signal Name	Pin#	Signal Name
1	GND	2	DCUTCK
3	GND	4	DCUTMS
5	GND	6	DCUTDI
7	GND	8	!DCUTRST
9	GND	10	N.C.
11	GND	12	!RESET
13	GND	14	FLMD0
15	GND	16	!DCUTRDY
17	GND	18	DCUTDO
19	GND	20	VDD

FlexRay A – 9 pins DB9F connector J12

Pin#	Signal Name	Description
2	BL	FlexRay Negative
3	GND	
7	BP	FlexRay Positive

FLX0TXDA - P1_11 pin 70 of UPD70F4010
 FLX0RXDA - P1_10 pin 71 of UPD70F4010
 FLX0TXENA - P1_9 pin 72 of UPD70F4010

J9 - Configuration of FlexRay A mode

Section	Signal Name	STATE	Description
1-2	BGE	ON	Bus Guardian Enable internal pull-down
3-4	STBN	OFF	low power mode; internal pull-down
5-6	EN	ON	Enabled; internal pull-down
7-8	WAKE	-	WAKE pin*

* Please refer to http://www.nxp.com/documents/data_sheet/TJA1080.pdf

FlexRay B – 9 pins DB9F connector J12

Pin#	Signal Name	Description
2	BL	FlexRay Negative
3	GND	
7	BP	FlexRay Positive

FLX1TXDB - P1_13 pin 67 of UPD70F4010
 FLX1RXDB - P1_12 pin 68 of UPD70F4010
 FLX1TXENB - P1_15 pin 65 of UPD70F4010

J11 - Configuration of FlexRay B mode

Section	Signal Name	STATE	Description
1-2	BGE	ON	Bus Guardian Enable internal pull-down
3-4	STBN	OFF	low power mode; internal pull-down
5-6	EN	ON	Enabled; internal pull-down
7-8	WAKE	-	WAKE pin*

* Please refer to http://www.nxp.com/documents/data_sheet/TJA1080.pdf

CAN0 – 9 pins DB9F connector J12

Pin#	Signal Name	Description
2	CAN L	
3	GND	
7	CAN H	

FCN0TX - P04 pin 30 of UPD70F4010
FCN0RX - P05 pin 31 of UPD70F4010
FCN0INH P0_13 pin 42 of UPD70F4010
FCN0RM P0_14 pin 41 of UPD70F4010

- *FCN0INH - LOW activate NORMAL mode
- *FCN0RM - LOW - activate READ ONLY MODE
- *Termination Jumper JP13.

CAN1 – 9 pins DB9F connector J13

Pin#	Signal Name	Description
2	CAN L	
3	GND	
7	CAN H	

FCN1TX - P07 pin 33 of UPD70F4010
FCN1RX - P06 pin 32 of UPD70F4010
FCN1INH P0_15 pin 40 of UPD70F4010
FCN1RM P0_12 pin 39 of UPD70F4010

- *FCN1INH - LOW activate NORMAL mode
- *FCN1RM - LOW - activate READ ONLY MODE
- *Termination Jumper JP16.

UART– 9 pins DB9F connector J16

Pin#	Signal Name	Description
2	TX RS	14 pin MAX202SA
3	RX RS	13 pin MAX202SA
5	GND	
1	loopback	
6	loopback	
4	loopback	

URTE7TX - P2_1 pin 119 of UPD70F3783GF.
URTE7RX - P2_2 pin 64 of UPD70F3783GF.
UART– 9 pins DB9F connector J17

Pin#	Signal Name	Description
2	TX_RS	7 pin MAX202SA
3	RX_RS	8 pin MAX202SA
5	GND	
1	loopback	
6	loopback	
4	loopback	

URTE3TX - P3_7 pin 60 of UPD70F3783GF.
 URTE3RX - P3_8 pin 59 of UPD70F3783GF.

LIN 1- 3 pin connectors J14

Pin#	Signal Name	Description
3	+VP	
2	LIN	
1	GND	

*Termination Jumper JP17.

LIN 2- 3 pin connectors J19

Pin#	Signal Name	Description
3	+VP	
2	LIN	
1	GND	

*Termination Jumper JP19.

Unused Pin Headers

J1

Pin#	Signal Name	Pin#	Signal Name
1	P21_8	2	P12_11
3	P12_9	4	P12_10
5	P12_8	6	P12_14
7	P21_7	8	P12_15
9	P12_6	10	!CS4
11	P12_5	12	!CS3
13	P12_4	14	P12_7
15	P3_2	16	P12_12
17	P10_15	18	P3_0
19	P10_14	20	GND

J2

Pin#	Signal Name	Pin#	Signal Name
1	P10_9	2	P10_11
3	+P10_8	4	P10_12
5	P10_7	6	P10_13
7	P10_6	8	P10_10
9	P3_4	10	P3_5
11	P0_1	12	P1_14
13	LED_7SEG_E	14	LED_7SEG_G
15	LED_7SEG_D	16	LED_7SEG_F
17	P0_0	18	N.C
19	P0_3/MODE1	20	GND

J3

Pin#	Signal Name	Pin#	Signal Name
1	VCPC1IN	2	VCPC0IN
3	P11_0	4	P11_1
5	P11_2	6	P11_3
7	P11_4	8	P11_5
9	P11_6	10	P11_7
11	P1_1	12	P1_2
13	P1_3	14	P1_4
15	P1_5	16	P1_6
17	P1_7	18	P1_8
19	-	20	GND

J4

Pin#	Signal Name	Pin#	Signal Name
1	P12_13	2	P12_3
3	P12_2	4	P12_1
5	P12_0	6	A18
7	WAKE	8	P21_6
9	P0_2	10	P27_4
11	P3_3	12	P2_0
13	P3_1	14	ADCA015
15	ADCA014	16	ADCA013
17	ADCA012	18	ADCA011
19	ADCA010	20	GND

J5

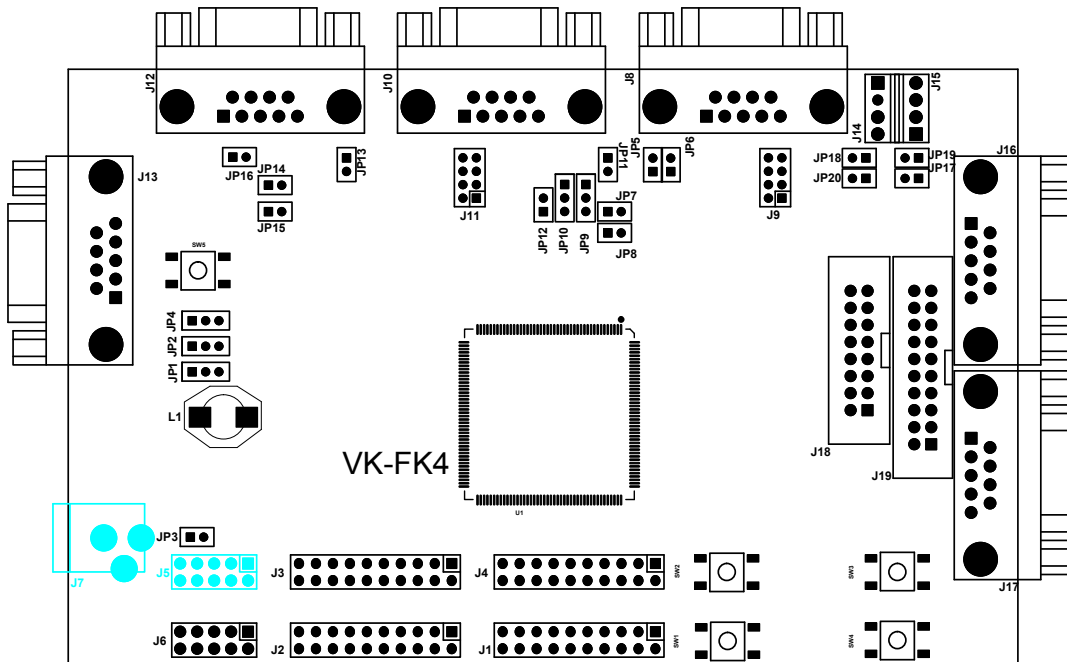
Pin#	Signal Name	Pin#	Signal Name
1	-	2	P27 3
3	-	4	-
5	-	6	-
7	REG 5V	8	REG VDD
9	+VP	10	GND

J6

Pin#	Signal Name	Pin#	Signal Name
1	LED_7SEG_C	2	LED_7SEG_B
3	LED_7SEG_DP	4	P4_9
5	P4_10	6	LED_7SEG_A
7	P4_8	8	P4_11
9	-	10	GND

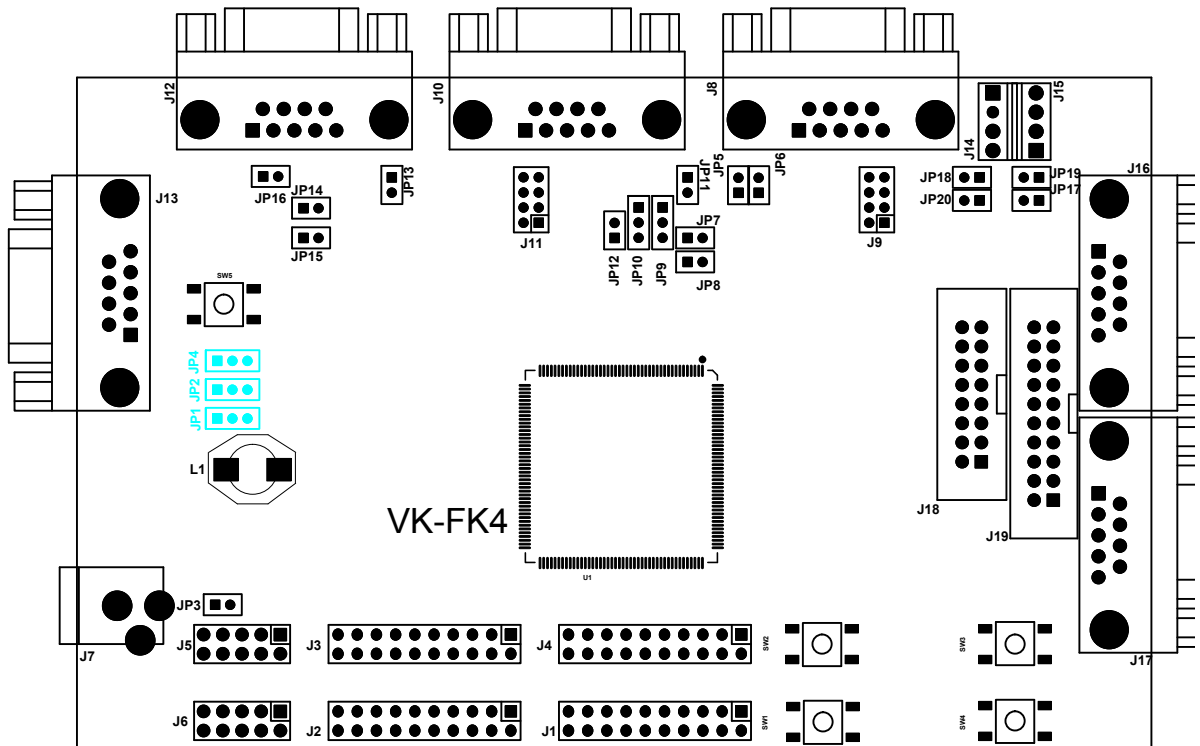
3.3 Jumper's Configuration

3.3.1 DC/DC Converter power source



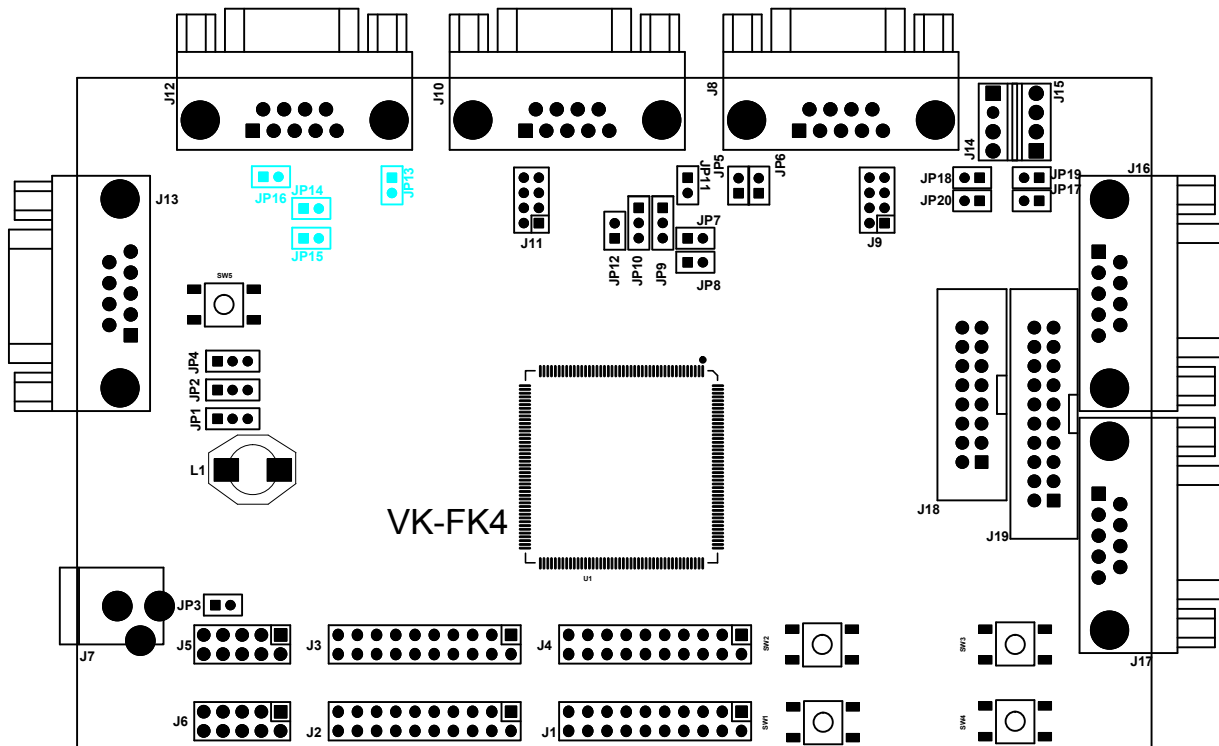
VK-FK4		DC/DC Converter Power Source
WARNING - ONLY ONE CONNECTION MUST BE ACHIEVED AT THE SAME MOMENT		
J7	--	Power Jack
J5	--	Pin Heaser 2x5 – pin 9 Note that there is no reverse protection when use J5

3.3.2 System power source



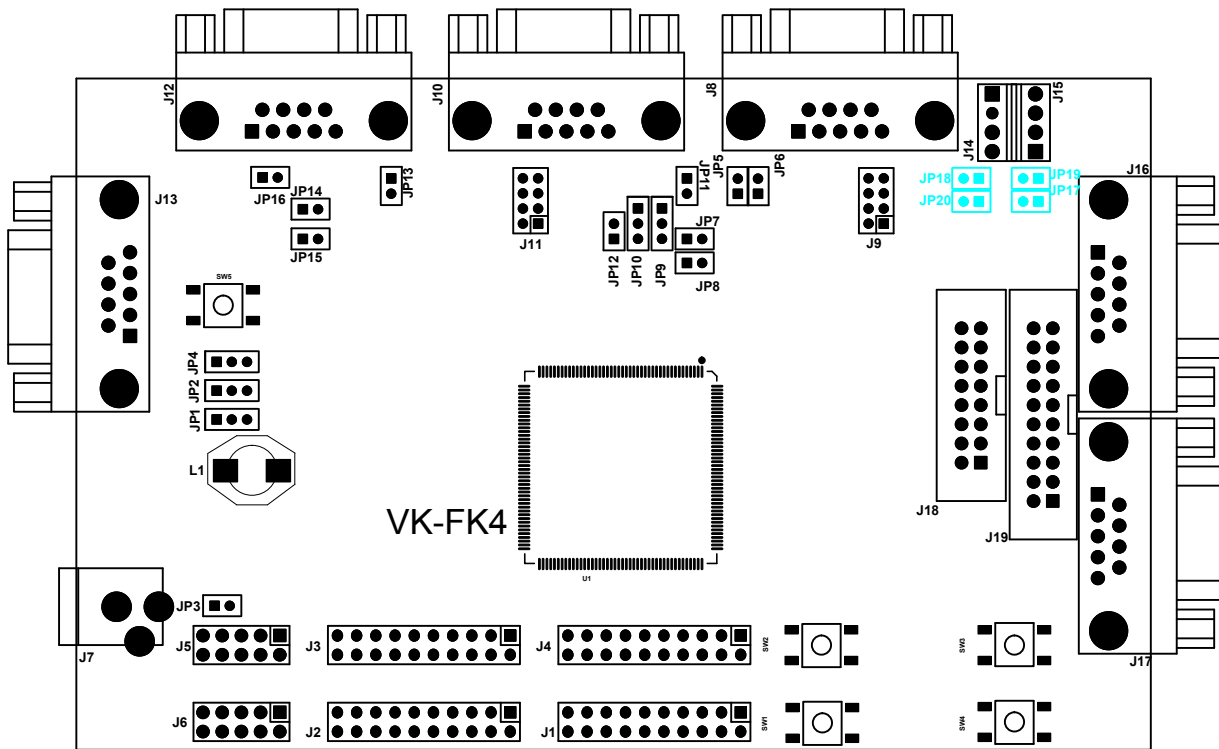
VK-FK4		VDDIO, VDD5V and VDD Configuration
WARNING !!! PLEASE MAKE SURE THAT ONLY ONE CONNECTION IS ACHIEVED AT THE SAME MOMENT		
	JP4	VDDIO CONNECTED TO REG_VDD (+3,3V)
	JP2	VDD5V CONNECTED TO REG_5V (+5,0V)
	JP1	VDD CONNECTED TO REG_VDD (+3,3V)

3.3.3 CAN Termination and Interconnection



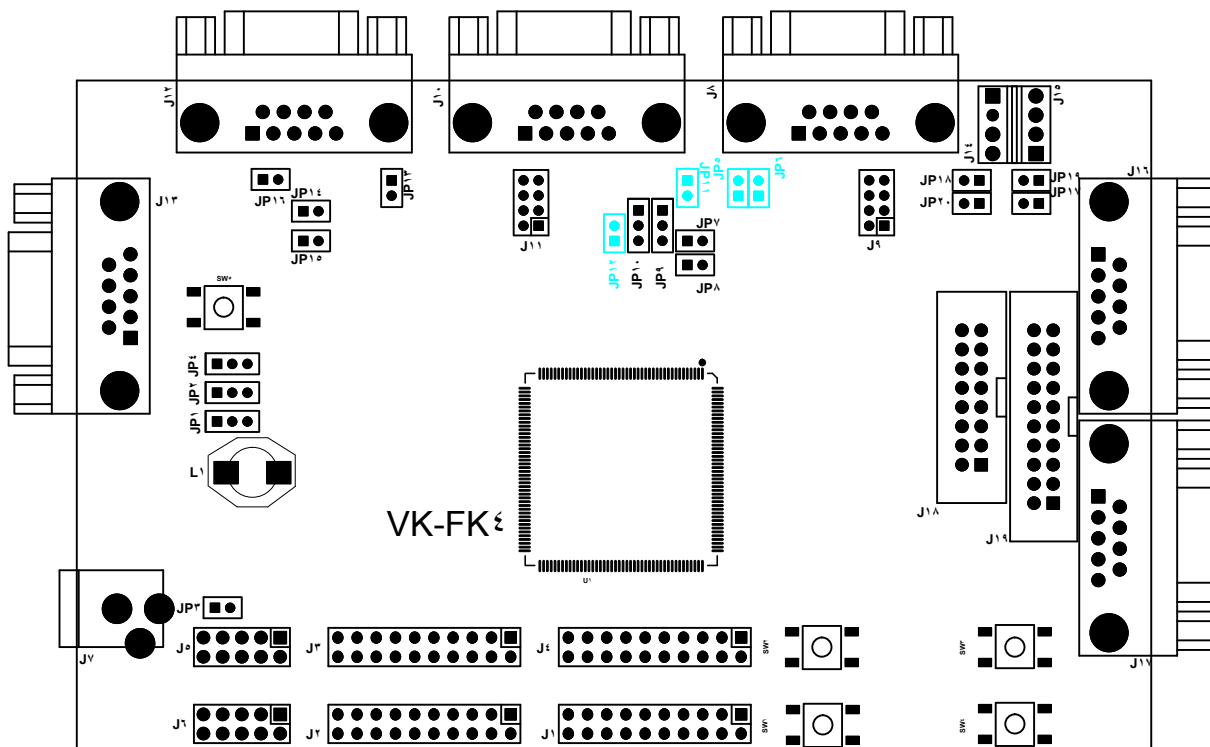
VK-FK4		CAN TERMINATION AND INTERCONNECTION
JP13	ON	CAN 0 TERMINATION IS ON
JP16	ON	CAN 2 TERMINATION IS ON
JP14/JP15	ON	CAN 0 CONNECTED TO CAN 1

3.3.4 LIN Termination and Supply



VK-FK4 LIN TERMINATION AND POWER SUPPLY		
JP18	ON	LIN 1 POWER SUPPLY OUT VIA J14/3
JP17	ON	LIN 1 TERMINATION IS ON
JP20	ON	LIN 0 POWER SUPPLY OUT VIA J15/3
JP19	ON	LIN 0 TERMINATION IS ON

3.3.5 FlexRay Termination



VK-FK4		FlexRay TERMINATION AND INTERCONNECTION
JP5&JP6	ON	FLEXRAY A TERMINATION ON
JP11&JP12	ON	FLEXRAY B TERMINATION ON

Interconnection between Channel A and Channel*

- ON JP7
- ON JP8
- ON 3-2 JP9
- ON 3-2 JP10

Chapter 4: On-Chip Debugging and Flash Program

4.1 OCD via Minicube2

Minicube2 can be connected to J18 and Renesas Electronics Flash Programmer 2.00 can be used as Flash programming tool.

Please use SIO-CH0 Interface.

*note E1 is not working with the same environment.

4.2 OCD via E1 Debugger

Use adapter board and cable supplied with the VK-FK4 board and connect to E1 interface connector J19.

Chapter 5: VK-FK4 Installation and Operation

Getting started

tbd

Chapter 6: Hardware Installation

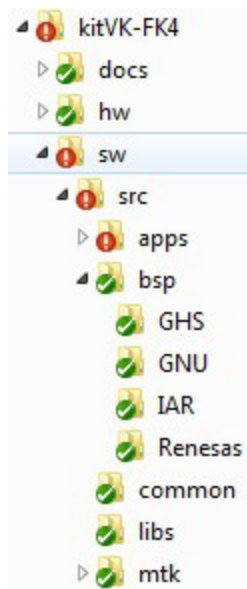
tbd

Chapter 7: Software Installation

This manual is not intended to guide you through installation procedures of any development or application software. Please refer to the relevant sources.

Chapter 8: Demo Projects

The available projects are prepared to compile with **IAR**, **GHS**, **GNU** and **Cubesuit+** Tool chains



The projects are located in folder **apps**. Each of them follows the organization:

<Project name>\app	- demo project's source files
<Project name>\prj\<tool chain>	- tool chain's project file
workspace\<tool chain>	- tool chain's workspace file. It includes all demo projects for the tool chain.

Folder **bsp** contains VK-FK4 board support package for multitask kernel.

bsp\<tool chain>	- tool chain's entry, vector, linker script files.
------------------	--

Folder **common** contains header and source files with useful macros and frequently used functions.

Folder **lib** is reserved for future library development.

Folder **mtk** contains headers and sources of the multitask kernel.

8.1 Test of external SRAM

General introduction

This test can be launched from **memtest** demo project and performs 3 tasks.

- Test the data bus wiring in entire memory region by performing a walking 1's.

- Test the address bus wiring in entire memory region by performing a walking 1's.
- Test the integrity of a physical memory device by performing an increment/decrement test over the entire region. In the process every storage bit in the device is tested as a zero and a one.

Sample Programs overview

The test is performed in infinite loop, therefore if the test keep running, 'r' will appear on the 7segment display. If the test fail 'E' will be displayed.

8.2 Periphery Test

General introduction.

This test can be launched from **periphery_test** demo project and checks the physical wiring between MCU and the periphery:

- UART
- LEDs
- Buttons
- ADC
- 7 segment display

Sample Programs overview

All the periphery works in real time. There is no matter the order of events occurrence. The reaction of the system is enough instantaneous from tester's point of view.

- **UART**: performs echo on port UART A (URTE3). When this port is connected to the COM port of the computer and if it's set up with 38400 bps, 8 bit data, No parity, 1 stop, the comport application (Terminal, PUTTY, Hyper terminal, and so on) should read the same data that was sent.
- **LEDs & Buttons**: They work in cooperation. When some of the buttons (SW1 - SW4) is pressed some of the LEDs (LD4 - LD7) lights up. The relation between button and LED is as follows: (SW1 - LD4, SW2 - LD5, SW3 - LD7, SW4 – LD6).
- **7 Segment & ADC**: also work together. ADC reads the voltage from RP1 and 7 segment shows that voltage with 330 mV accuracy. Constraint is simple: display can show only 10 different digits, and supply voltage is 3,3 V. Accuracy = voltage / digits. When RP1 turns from left to right the digit on the display should increment from 0 to 9. Blinking of the dot segment indicate proper MCU operation. Blink must be with frequency 0,5 Hz. (1s on, 1s off).

8.3 Other Tests

General introduction.

To this group belongs: **can_test** and **lin_test** demo projects. Both do the same thing like periphery test and include the same periphery except for the UART. The difference is in changed data path when MCU communicates with ADC, buttons and leds. Once the conversation pass through the lin interface (**lin_test**) and next time it is through the can (**can_test**).

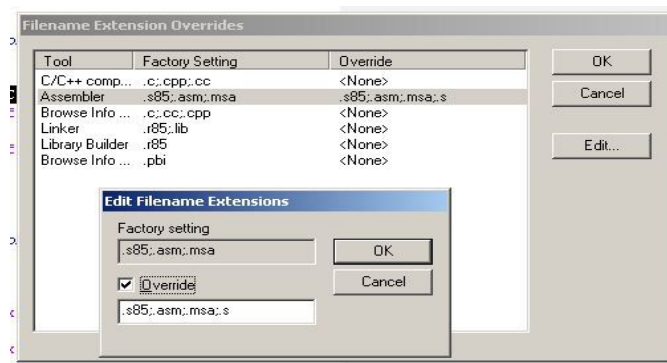
Sample Programs overview

Connect J14 with J15 before performing of **lin_test**, or put jumpers on J14 & J15 before starting the **can_test**. Leds and 7 segment display react the same way to the buttons and the turning of RP1, like in periphery test. If the connection between LIN connectors is removed while **lin_test** is running leds, buttons and 7 segment display stops working, only dot keep blinking. The same is true for the **can_test** if connection between cans is removed. If the connection is back both tests work properly just like in periphery test.

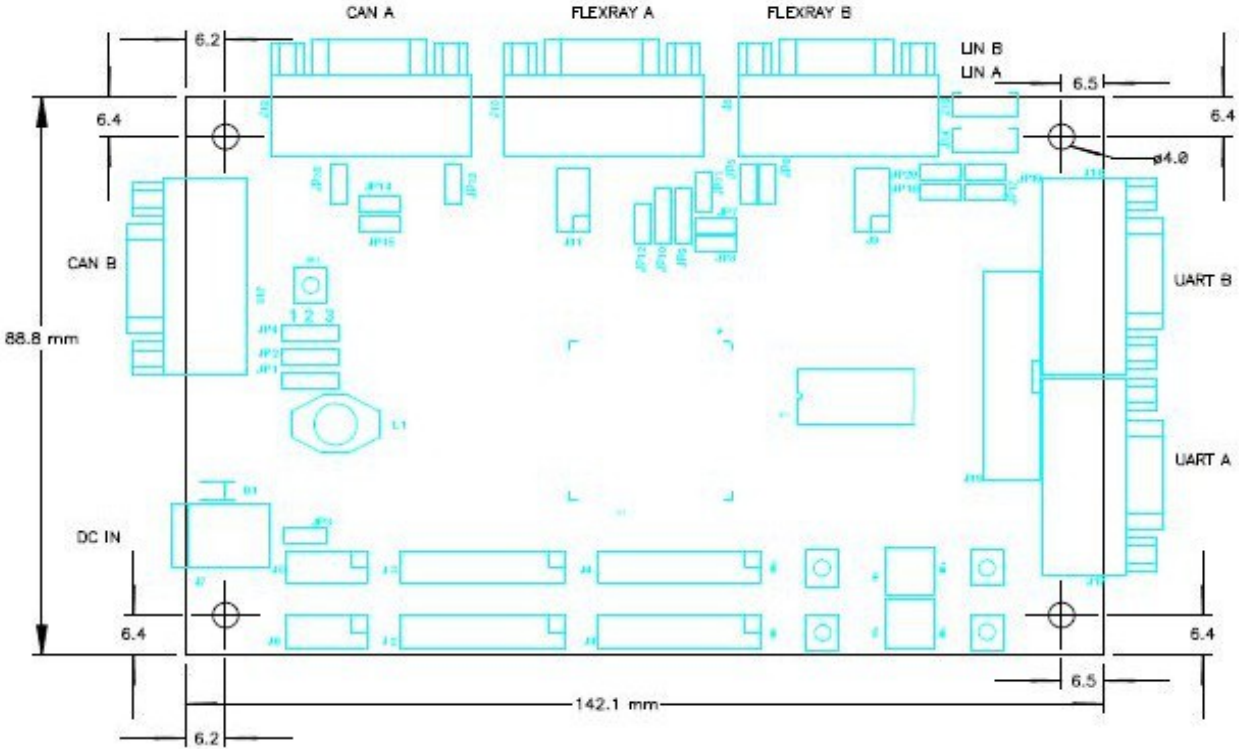
Chapter 9: Setting IAR Workbench

9.1 Setting IAR V850 Assembler for use with the demo projects

Go to Tools/Filename extensions and Assembler/Edit.
Update the list of assembler files with .s extension.



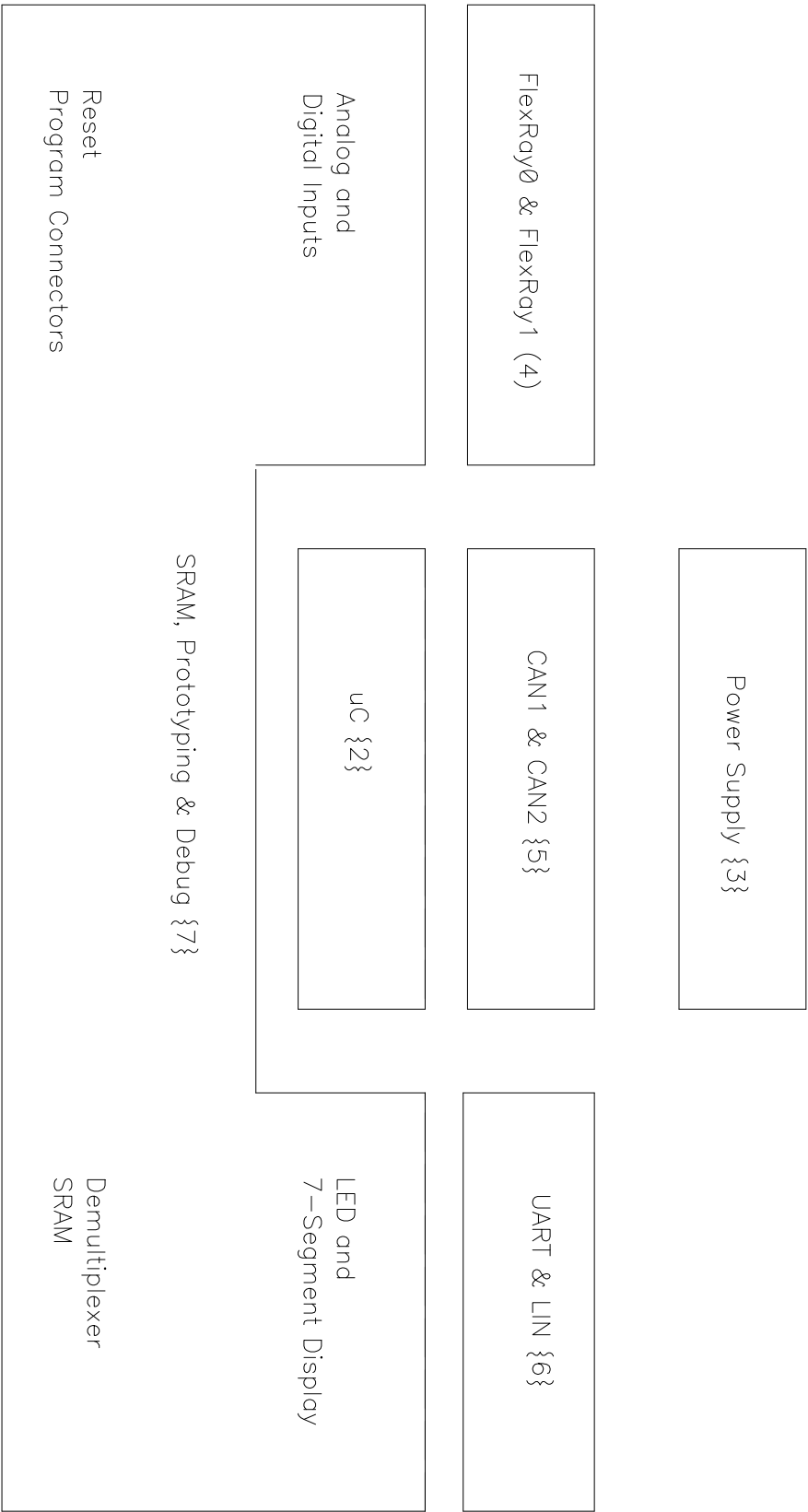
Chapter 10: Mechanical Dimmensions



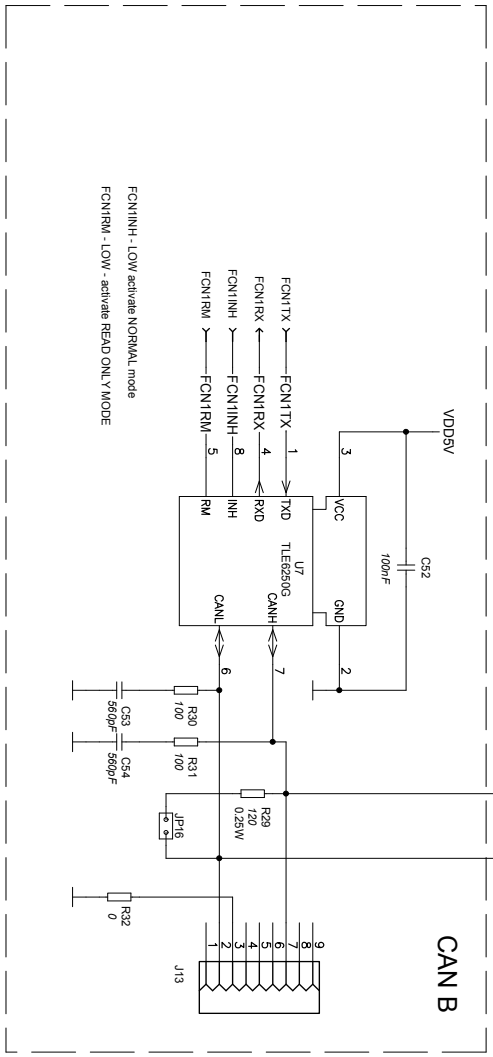
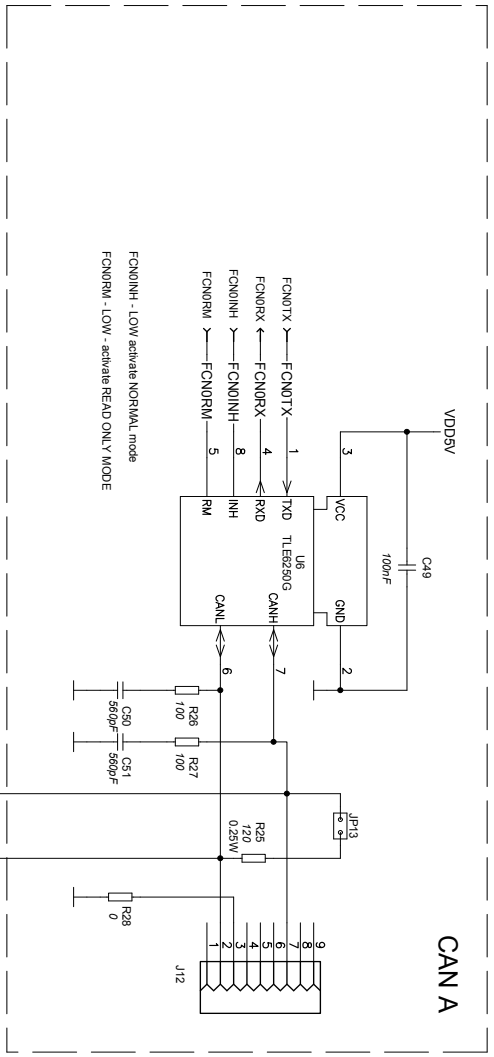
All measures are in mm.

Chapter 11: Reference Designators

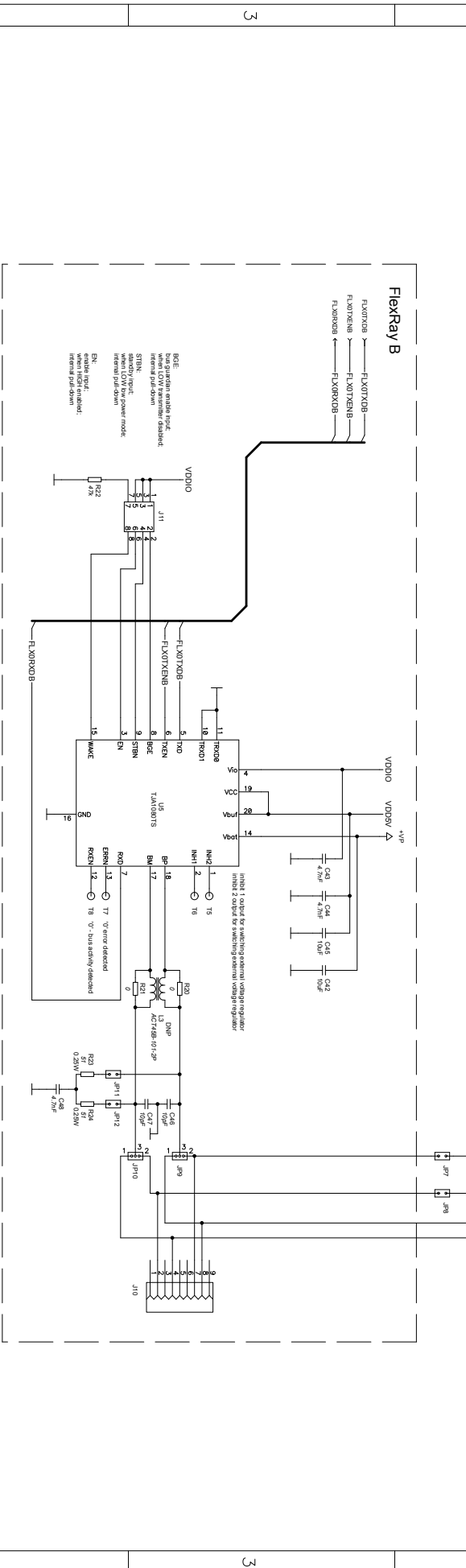
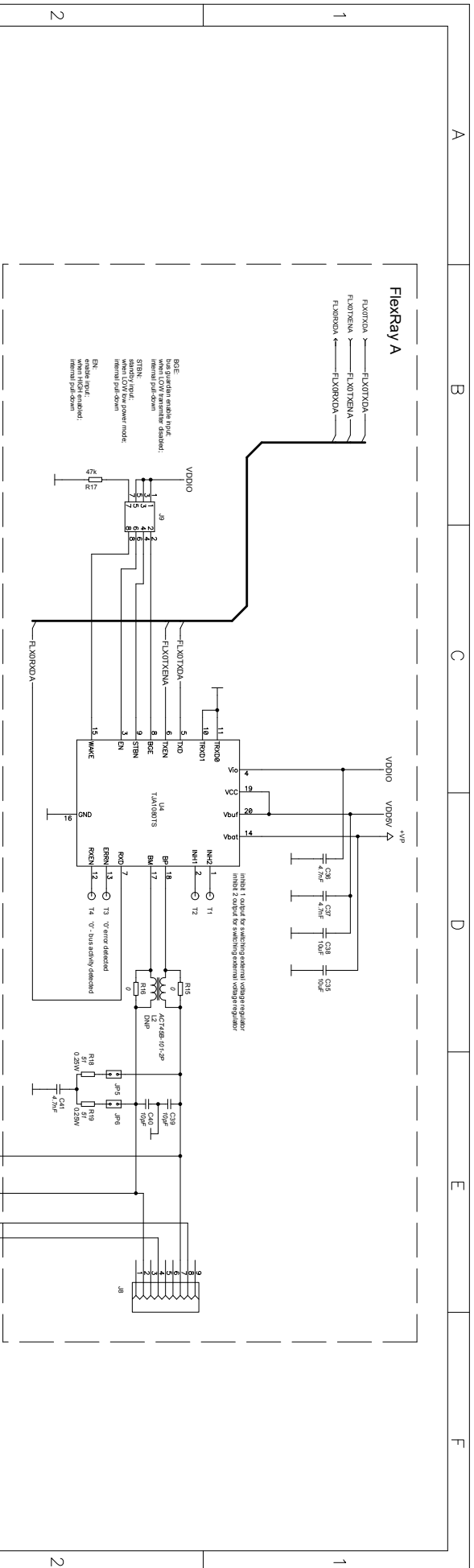
Chapter 12: Schematics



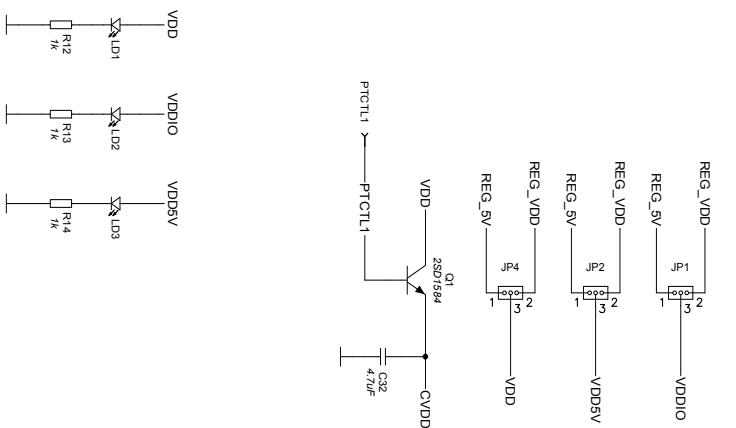
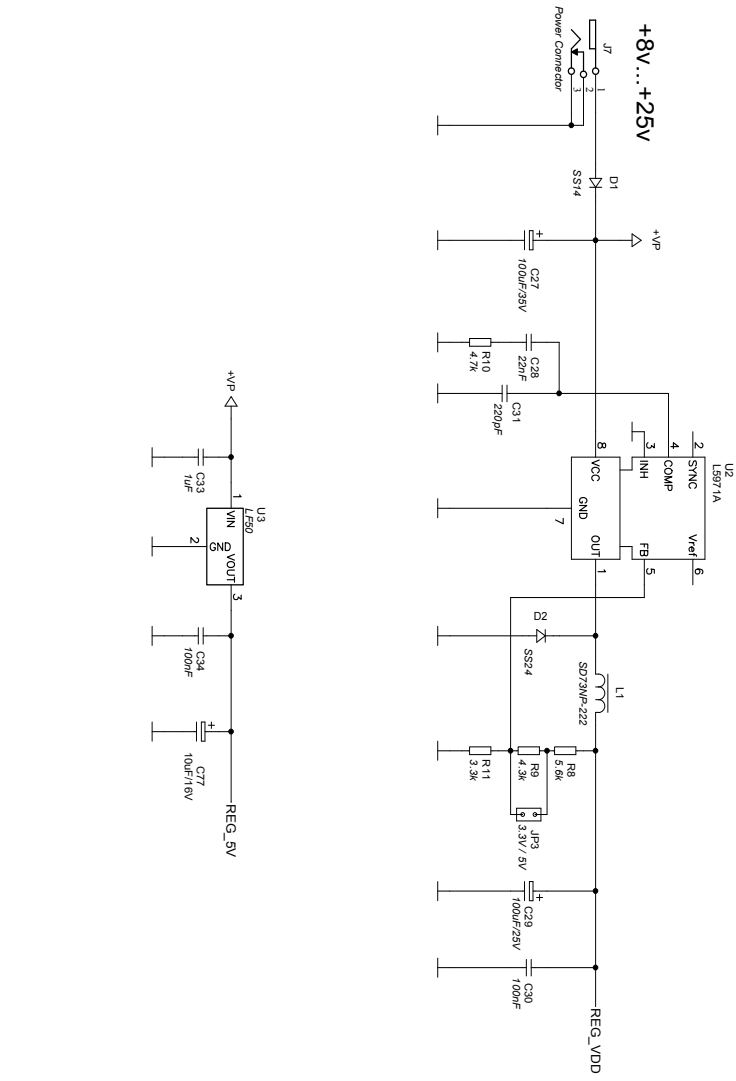
Title		VK-Fx4	
Size	Number	VK-Fx4 - uPD70F4010	Rev
A2			1.0
Date	{Date}	Drawn by D.Todorov	
Filename	vk_fk4_rev1.sch	Sheet 1	of 7



Title		VK-FX4		CAN	
Size	Number	VK-FX4 - uP(D7)4010		Rev	1.0
Date	(Date)	VK_K4_rev1_sch		Drawn by	D.Todorov
Filename		VK_K4_rev1_sch		Sheet	5 of 7

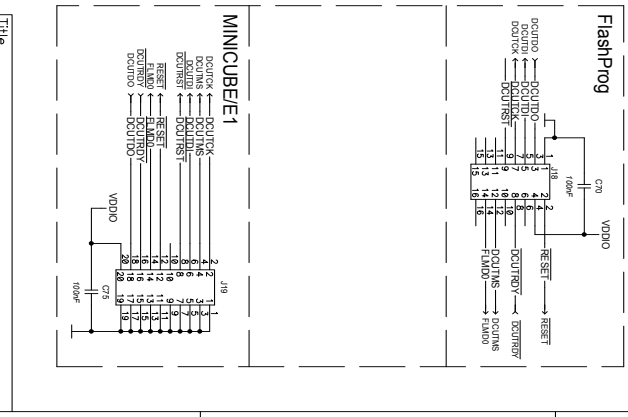
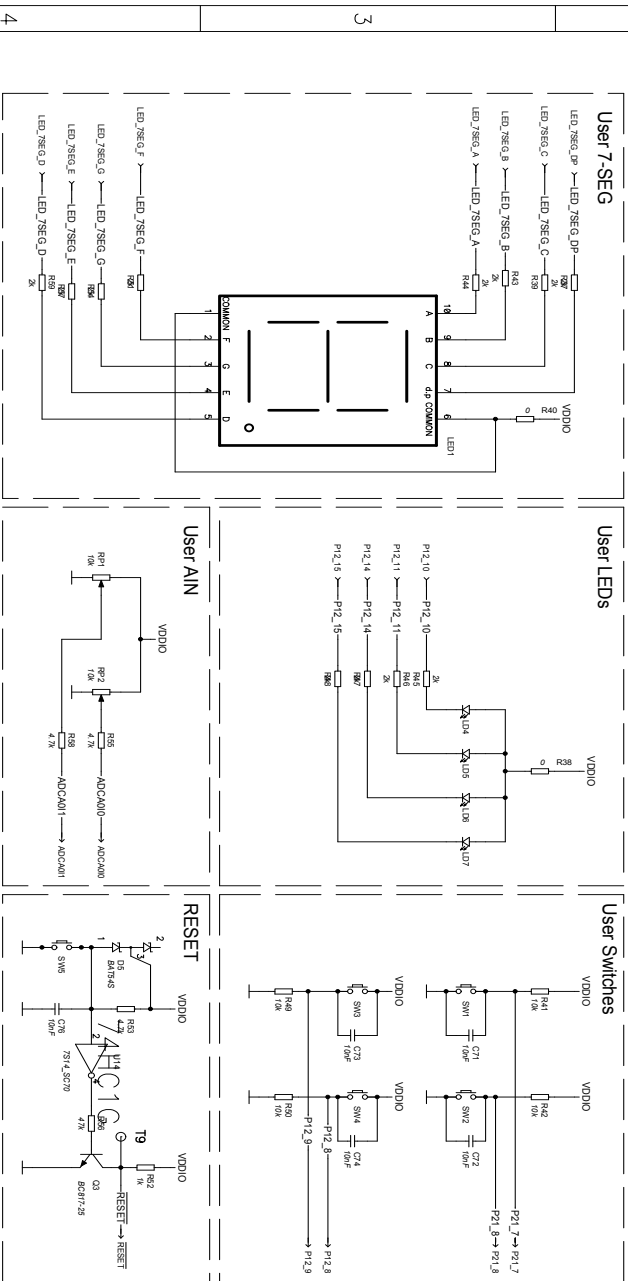
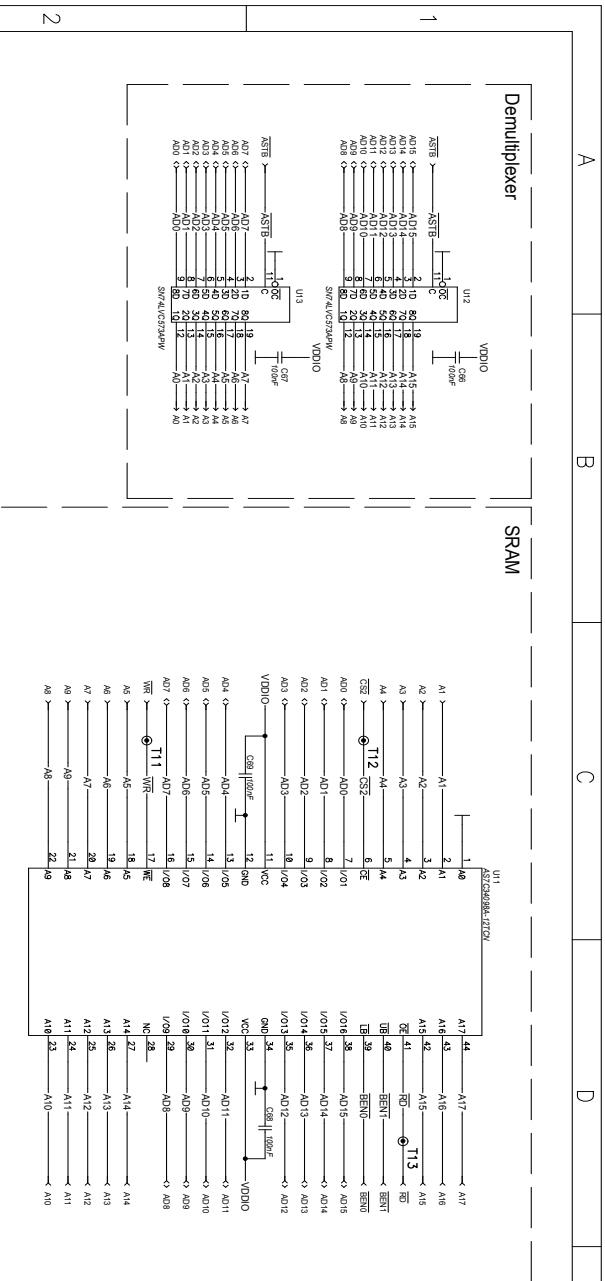


Title	VK-Fx4	FlexRay
Size	A2	Rev 1.0
Number	VK-Fx4 - uPD70F4010	Drawn by D. Todorov
Date	[Date]	Sheet 4 of 7
Filename	VK_Fx4_rev1.sch	



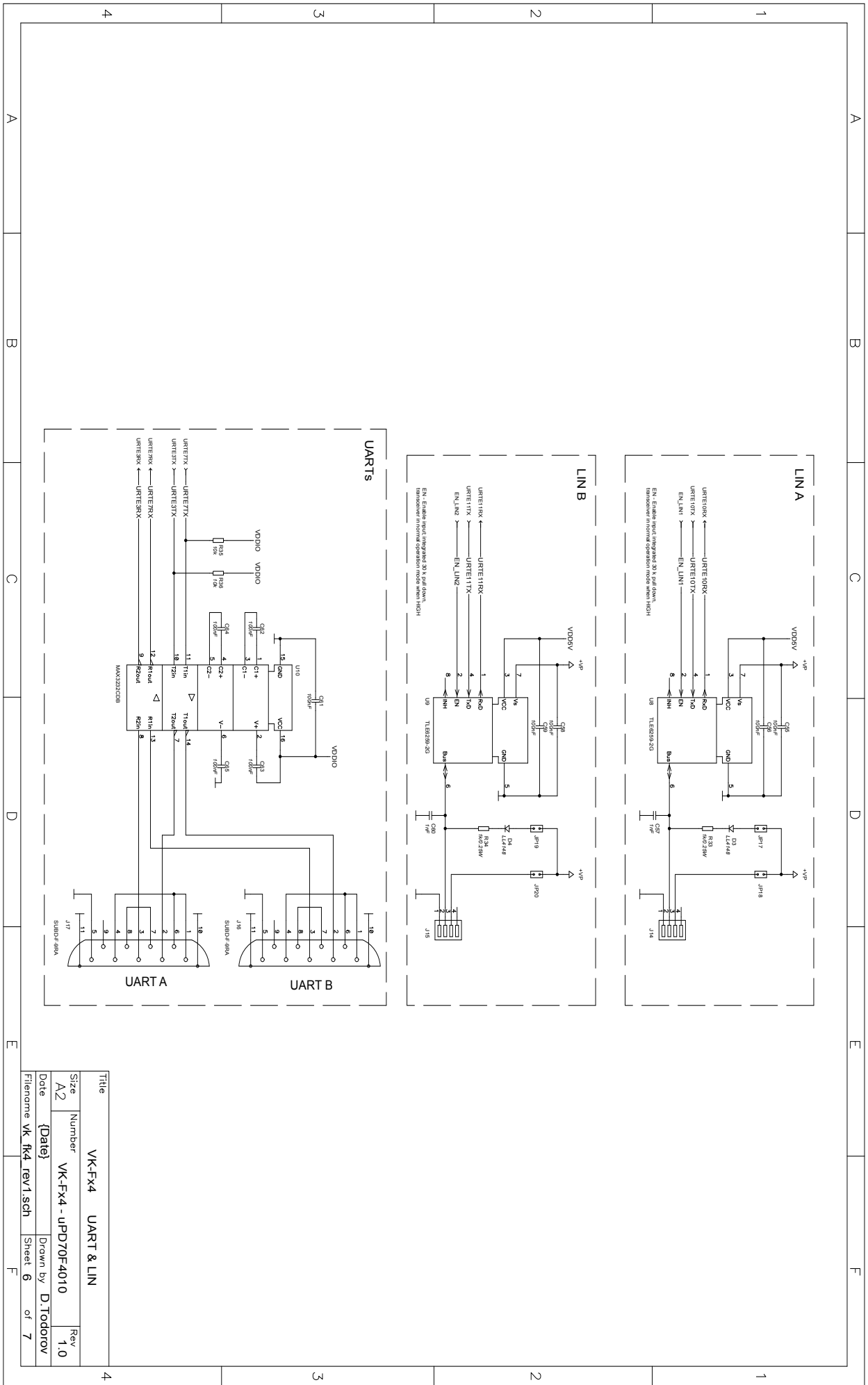
Ref Des	Device (Type)	Package (GND)	VDDIO
U12	SN74HCS73A(FWI)	ESQP20	18 20
U13	SN74HCS73A(FWI)	ESQP20	18 20
U14	7514_S070	SC70	5 5

Title		VK-F04	Power Supply
Size	Number	VK-F04	upDF04-010
A3	1.0		
Date	Drawn by	Daniel	D.Todorov
Filename	vk_fk_rev1.sch	Sheet 3	of 7

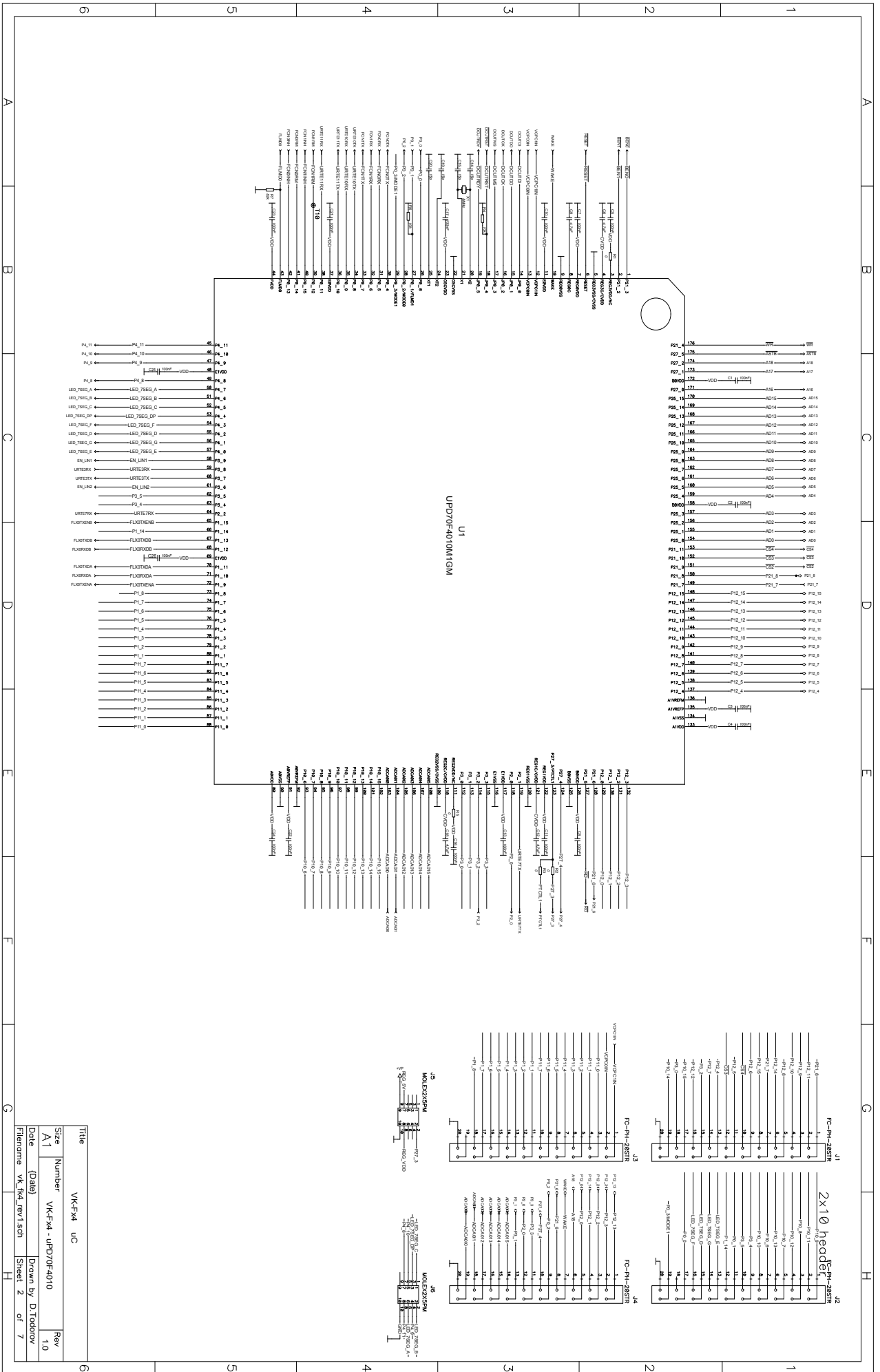


4	A	B	C	D	E	F
4	A	B	C	D	E	F
3	A	B	C	D	E	F
2	A	B	C	D	E	F
1	A	B	C	D	E	F

Title		VK-Fx4 SRAM, Prototyping & Debug	
Size	Number	Rev	
A2	VK-Fx4 - UPTD70F4010	1.0	
Date	{Date}	Drawn by	D.Todorov
Filename	Vk_fk4_rev1.sch	Sheet	7 of 7



Title		VK-FX4 UART & LIN	
Size	Number	VK-FX4 - uPD70F4010	Rev
A2			1.0
Date	{Date}	Drawn by	D.Todorov
Filename vk_fx4_rev1.sch		Sheet	6 of 7



Title	VK-FK4 UC
Size	A 1
Number	VK-FK4 - UPD70F4010
Date	(Date)
Drawn by	D.Todorov
Sheet	2 of 7
Rev	1.0

Chapter 13: Troubleshooting

Chapter 14: End